February 22, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
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Subject: Serial No. 10/029,622 12/31/01

Y.F. Lin, C.S. Lin, C.T. Hsieh,
H.C. Sung, J. Yeh

A METHOD TO FABRICATE A NON-SMILING EFFECT STRUCTURE IN SPLIT-GATE FLASH WITH SELF-ALIGNED ISOLATION

Grp. Art Unit: 2822

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 27, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Ackerman 2/27/02

U.S. Patent 5,447,884 to Fahey et al., "Shallow Trench Isolation with Thin Nitride Liner", discloses a method of forming shallow trench isolation by using a nitride liner with a thickness less than 5 nanometers (nm) in order to prevent the formation of unacceptable voids in the trench.

U.S. Patent 5,652,161 to Ahn, "Method of Making Split Gate Flash EEPROM Cell", discloses the use of a thick insulation film between the tunneling region and the channel region in an EEPROM split-gate flash memory cell in order to prevent the degradation of the tunnel oxide film due to the band-to-band tunneling and the secondary hot carriers which are generated by a high electric field formed at the overlap regions between the junction region and the gate electrode when programming and erasure operations are performed with high voltage.

U.S. Patent 5,597,751 to Wang, "Single-Side Oxide Sealed Salicide Process for EPROMS", shows a method of preventing shorting between a floating gate and a source/drain region of a substrate by depositing a thick spacer oxide layer on top of the floating gate and the source/drain region to a sufficient thickness such that electrical insulation is provided therebetween.

Sincerely,

Stephen B Ackerman

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